Serial Number: 09/551,027 Filing Date: April 17, 2000

CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH Title:

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# §112 Rejection of the Claims

Claims 25-26 and 34-40 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 25 has been amended to remove the limitation of forming second source/drain region layer "epitaxially," thereby overcoming the rejection of claims 25 and claims 26 and 34-40 depending directly or indirectly therefrom. Withdrawal of the rejection of these claims is therefore respectfully requested.

#### §102 Rejection of the Claims

Claims 20-21, 23-24, 27-28, 30, 32, 34-35, 37, 39, 41-42, 44, 46, 48-53 were rejected under 35 USC § 102(b) as being anticipated by Gotou (U.S. 5,001,526).

An anticipating reference must describe the patented subject matter with sufficient clarity and detail to establish that the subject matter existed and that its existence was recognized by persons of ordinary skill in the art. ATD Corp. v. Lydall, Inc., 48 USPQ2d 1321, 1328 (Fed. Cir. 1998). There must be no difference between the claimed invention and the reference disclosure, as viewed by one of ordinary skill in the art. Scripps Clinic & Research Foundation v. Genentech, Inc. 18 USPQ2d 1001, 1010 (Fed. Cir. 1991).

The Examiner has based the rejection in the alternative with respect to two different teachings in Gotou: (1) the prior art invention of Minegishi as described in the "Background of the Invention" section in col. 2, lines 12-50, and FIG. 2; and (2) the invention of Gotou as described in col. 2, line 55 and above, and FIG. 3(a) and above.

Applicant addresses these alternative rejections in turn below.

# (1) Minegishi invention of FIG. 2

The Minegishi invention is described in Gotou in col. 2, lines 12-50 and is illustrated in FIG. 2. Critical to the device of Minegishi is a p+-type implanted isolation region (70) formed in substrate (60). The implanted isolation region resides beneath doped polysilicon/cell plate

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(69) in the lower portion of the trench when the trench is filled. The function of the implanted isolation region is to prevent leakage of electric charges between storage electrodes (68). Col. 2, lines 33-35.

In contrast, Applicant's invention does not require such an isolation region, which makes for a simplified structure. Applicant has amended claims 20, 25, 41, 49, 51, 53 and 55 to clarify this point.

# (2) Gotou invention, FIG. 3(a) and above

The Gotou invention is directed to forming a DRAM cell using so-called "bonded wafer" technology, as described in col 4, line 41 through col. 5, line 9 and FIGS. 4A, 4B and 5. This technology involves forming layers on two separate substrates, interfacing the substrates, bonding them together, and then polishing one of the substrates to obtain the multi-layered structure (FIG. 6).

Examiner notes in his latest response that "the substrate 12 as shown in Figures 4A and 4B of Gotou is a *single substrate from which* a number of access transistors are formed thereon." While this may be true, the point Applicant was trying to make and emphasizes again here is that the method of Gotou requires starting with and using *two substrates* and then *bonding* them together to form a *single* substrate. This is in contrast to Applicant's invention, which starts with and uses only a *single substrate*. Applicant's claimed process does not include any steps involving bonding substrates together to form the single substrate, which makes for a more complicated and expensive device fabrication process.

Applicant has amended claims 20, 25, 41, 49, 51, 53 and 55 to emphasize this point by adding the limitation that the substrate used in the claimed methods is *unbonded*. Because the substrate of Gotou is clearly *bonded*, Gotou cannot be said to disclose this limitation of Applicant's invention.

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Examiner also notes in his latest response that the prior art of Minegishi as illustrated in FIG. 2 of Gotou shows a device formed on a single substrate 60. However, Applicant's invention as presently claimed is distinguishable from Minegishi because Applicant's invention does not include the implanted barrier layer critical to the operation of the semiconductor device of Minegishi, as explained above.

In view of the above, applicant respectfully requests the withdrawal of the rejection of claims 20-21, 23-24, 27-28, 30, 32, 34-35, 37, 39, 41-42, 44, 46, 48-53 as being anticipated under 35 USC § 102(b).

#### §103 Rejection of the Claims

Claims 22, 29, 31-32, 35, 38, 40, 43, 45, 47, 54-56 were rejected under 35 USC § 103(a) as being unpatentable over Gotou (U.S. 5,001,526) taken with Kimura et al.(U.S.5,177,576) ("Kimura"). The rejection is based on the presumption that claims 20-21, 23-24, 27-28, 30, 32, 34-35, 37, 39, 41-42, 44, 46, 48-53 were properly rejected under 35 USC § 102(b).

Applicant respectfully submits that the rejection of claims 20-21, 23-24, 27-28, 30, 32, 34-35, 37, 39, 41-42, 44, 46, 48-53 under 35 USC § 102(b) is overcome for the reasons explained above. Thus, the basis of the rejection of the above-cited claims under 35 USC § 103(a) no longer exists.

Applicant therefore respectfully requests that the obviousness rejection under 35 USC § 103(a) of the above-cited claims be withdrawn.

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#### Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612- 373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this <u>21st</u> day of <u>February</u>, 2002.

Name

y Moriatty

Signature